

REVISIONS															
LTR	DESCRIPTION										DATE (YR-MO-DA)				APPROVED
A	Change to figure 4. Editorial changes throughout.										88-11-08				M. A. Frye
B	Add devices 05 and 06. Technical and editorial changes throughout.										92-11-04				M.L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																																
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REV STATUS OF SHEETS				REV		B	B	B	B	B	B	B	B	B	B	B	B	B	B													
				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14													
PMIC N/A STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				PREPARED BY Greg A. Pitz					DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444																							
				CHECKED BY Ray Monnin																												
				APPROVED BY Michael A. Frye																												
				DRAWING APPROVAL DATE 87-09-25																												
				REVISION LEVEL B					SIZE A		CAGE CODE 67268		5962-87704																			
										SHEET 1 OF 14																						

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-87704	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	29C861	High performance CMOS 10-bit bus transceiver
02	29C863	High performance CMOS 9-bit bus transceiver
03	29C961	High performance CMOS 10-bit bus transceiver (rotated die) <u>1</u> /
04	29C963	High performance CMOS 9-bit bus transceiver (rotated die) <u>1</u> /
05	29C861A	High performance CMOS 10-bit bus transceiver
06	29C863A	High performance CMOS 9-bit bus transceiver

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range - - - - -	-0.5 V dc to +7.0 V dc
Input voltage range - - - - -	-0.5 V dc to 6.0 V dc
DC output voltage range - - - - -	-0.5 V dc to 6.0 V dc
DC output diode current: into output - - - - -	+50 mA
DC output diode current: out of output - - - - -	-50 mA
DC input diode current: into input - - - - -	+20 mA
DC input diode current: out of input - - - - -	-20 mA
DC output current per pin: I_{SINK}	
Device types 01-04 - - - - -	+48 mA ($2 \times I_{OL}$)
Device types 05, 06 - - - - -	+100 mA ($2 \times I_{OL}$)
DC output current per pin: I_{SOURCE}	
Device types 01-04 - - - - -	-30 mA ($2 \times I_{OH}$)
Device types 05, 06 - - - - -	-100 mA ($2 \times I_{OH}$)
Total dc ground current - - - - -	$(n \times I_{OL} + m \times I_{CCT})$ mA <u>2</u> /
Total dc V_{CC} current - - - - -	$(n \times I_{OH} + m \times I_{CCT})$ mA <u>2</u> /
Storage temperature range - - - - -	-65°C to +150°C
Maximum power dissipation P_D <u>3</u> / - - - - -	500 mW
Lead temperature (soldering, 10 seconds) - - - - -	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases K, L, and 3 - - - - -	See MIL-STD-1835
Junction temperature (T_J) - - - - -	+150°C

1/ Not available from an approved source of supply.

2/ n = number of outputs, m = number of inputs.

3/ For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ derate linearly at 10 mW/°C.

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1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	- - - - -	+4.5 V dc to +5.5 V dc
Minimum high-level input voltage (V_{IH})	- - - - -	2.0 V dc
Maximum low-level input voltage (V_{IL})	- - - - -	.8 V dc
Case operating temperature range (T_C)	- - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V V _{IN} = V _{IL} or V _{IH}	1, 2, 3	All	2.4		V
Low level output voltage	V _{OL}	V _{CC} = 4.5 V V _{IN} = V _{IH} or V _{IL}	1, 2, 3	01-04		0.5	V
				05,06			
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V I _{IN} = -18 mA	1, 2, 3	All		-1.2	V
Low level input current	I _{IL1}	V _{CC} = 5.5 V Input only	1, 2, 3	01-04		-10	μA
				05,06		-5	
	I _{IL2}			01-04		-5	μA
High level input current	I _{IH1}	V _{CC} = 5.5 V Input only	1, 2, 3	01-04		5	μA
				01-04		10	μA
	I _{IH2}			05,06		5	
Off-state leakage current	I _{OZH1}	V _{CC} = 5.5 V I/O port	1, 2, 3	01-04		15	μA
				01-04		20	μA
				05,06		10	
	I _{OZL1}			01-04		-15	μA
	I _{OZL2}			01-04		-20	μA
				05,06		-10	
Static supply current	I _{CCQ}	V _{CC} = 5.5 V Outputs open	1,2,3	01-04		160	μA
				05,06		1.5	mA
	I _{CCT}					1.5	mA/bit
		V _{IN} = 3.4 V				1.5	mA/bit
		Data input				1.5	mA/bit
		OER1				3.0	mA/bit
		OER2				3.0	mA/bit
		OET1				3.0	mA/bit
		OET2				3.0	mA/bit

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
Output short circuit current	I _{SC}	V _{CC} = 5.5 V V _{OUT} = 0 V <u>1</u> /	1, 2, 3	ALL	-60		mA
Functional testing		See 4.3.1d	7, 8	All			
Input capacitance	C _{IN}	See 4.3.1c	4	All		16	pF
Output capacitance	C _{OUT}	See 4.3.1c	4	All		20	pF
I/O capacitance	C _{I/O}	See 4.3.1c	4	All		20	pF
Propagation delay from Ri to Ti or Ti to Ri	t _{PLH}	See figure 4 C _L = 50 pF R ₁ = 500Ω R ₂ = 500Ω	9,10,11	01-04		12	ns
				05,06		8	
Propagation delay from Ri to Ti or Ti to Ri	t _{PHL}		9,10,11	01-04		12	ns
				05,06		9	
Output enable time OET to Ti or OER to Ri	t _{PZH}		9,10,11	01-04		16	ns
				05		11	
				06		11.5	
Output enable time OET to Ti or OER to Ri	t _{PZL}		9,10,11	01-04		16	ns
				05,06		13.5	
Output disable time OET to Ti or OER to Ri	t _{PHZ}		9,10,11	01-04		16	ns
				05		10	
				06		11	
Output disable time OET to Ti or OER to Ri	t _{PLZ}		9,10,11	01-04		16	ns
				05		11	
				06		12	

1/ Not more than one output shorted at a time. Duration should not exceed 100 ms.

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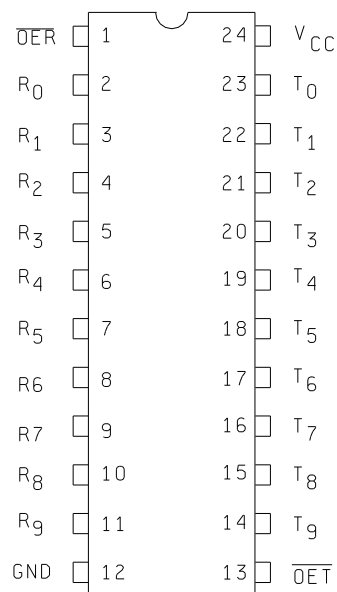
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Device types 01 and 05

Case outlines K and L



Device types 01 and 05

Case outline 3

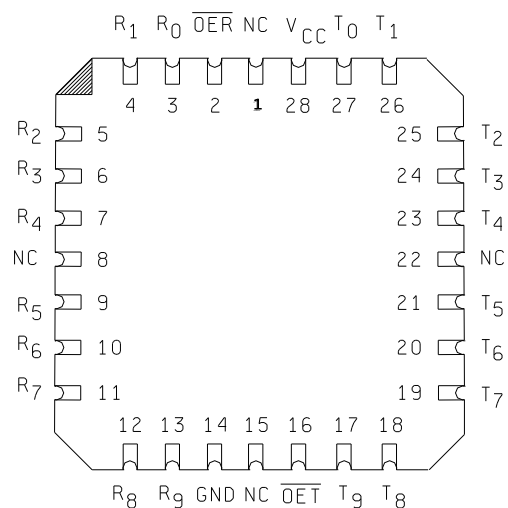


FIGURE 1. Terminal connections.

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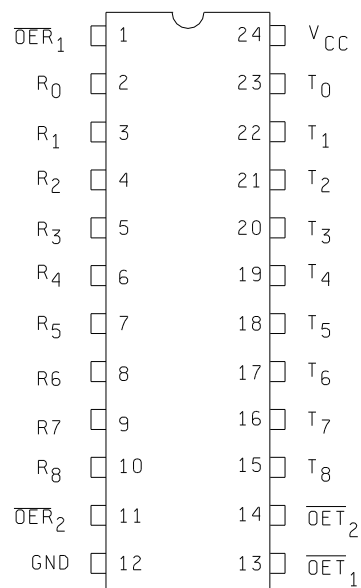
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Device types 02 and 06

Case outlines K and L



Device types 02 and 06

Case outline 3

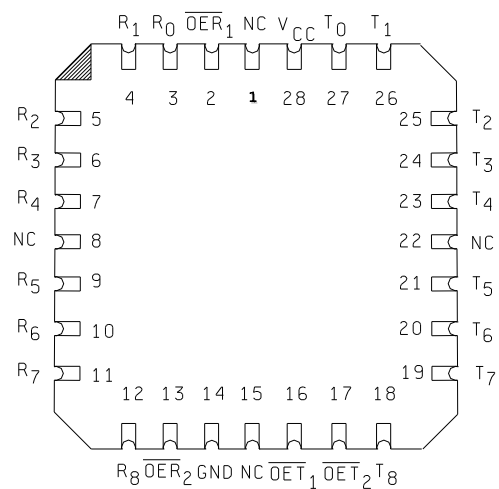


FIGURE 1. Terminal connections - Continued.

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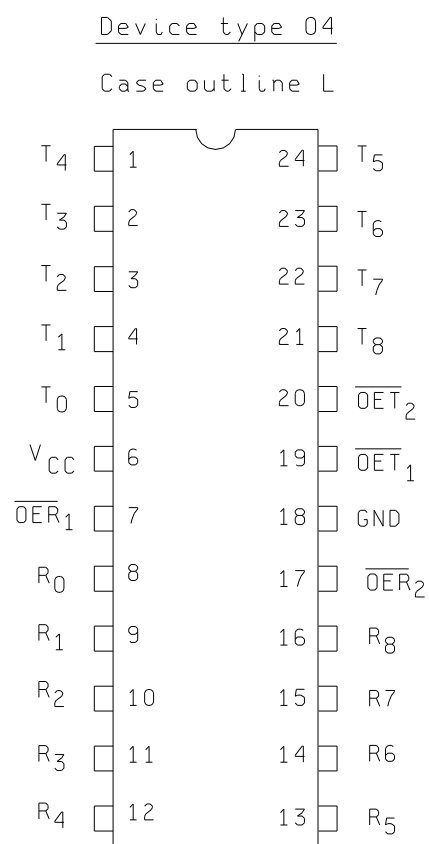
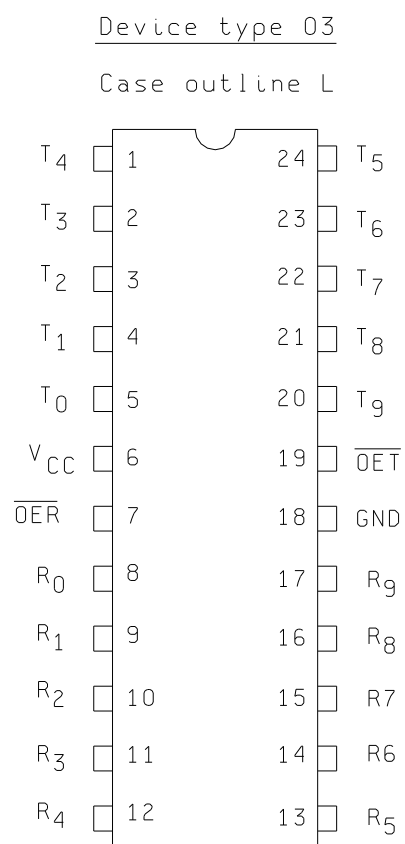


FIGURE 1. Terminal connections - Continued.

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Device types 01, 03, and 05

Inputs				Outputs		Function
$\overline{\text{OET}}$	$\overline{\text{OER}}$	R_i	T_i	R_i	T_i	
L	H	L	N/A	N/A	L	Transmit
L	H	H	N/A	N/A	H	Transmit
H	L	N/A	L	L	N/A	Receive
H	L	N/A	H	H	N/A	Receive
H	H	X	X	Z	Z	Hi-Z

Device types 02, 04, and 06

Inputs						Outputs		Function
$\overline{\text{OET}}_1$	$\overline{\text{OET}}_2$	$\overline{\text{OER}}_1$	$\overline{\text{OER}}_2$	R_i	T_i	R_i	T_i	
L	L	H	X	L	N/A	N/A	L	Transmit
L	L	X	H	L	N/A	N/A	L	Transmit
H	X	L	L	N/A	L	L	N/A	Receive
X	H	L	L	N/A	L	L	N/A	Receive
L	L	H	X	H	N/A	N/A	H	Transmit
L	L	X	H	H	N/A	N/A	H	Transmit
H	X	L	L	N/A	H	H	N/A	Receive
X	H	L	L	N/A	H	H	N/A	Receive
H	X	H	X	X	X	Z	Z	Hi-Z
X	H	X	H	X	X	Z	Z	Hi-Z

H = High

L = Low

Z = High impedance

X = Don't care

N/A = Not applicable

FIGURE 2. Truth tables.

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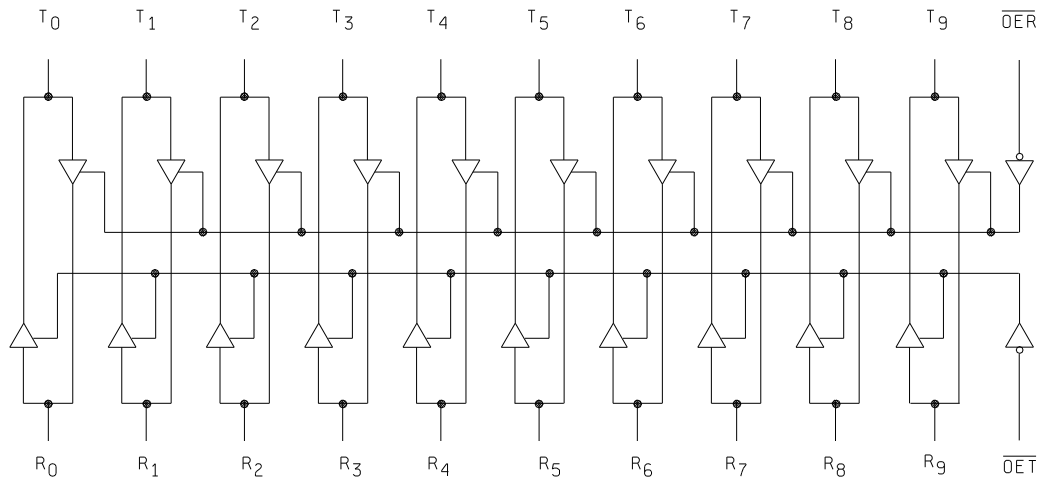
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Device types 01, 03, and 05



Device types 02, 04, and 06

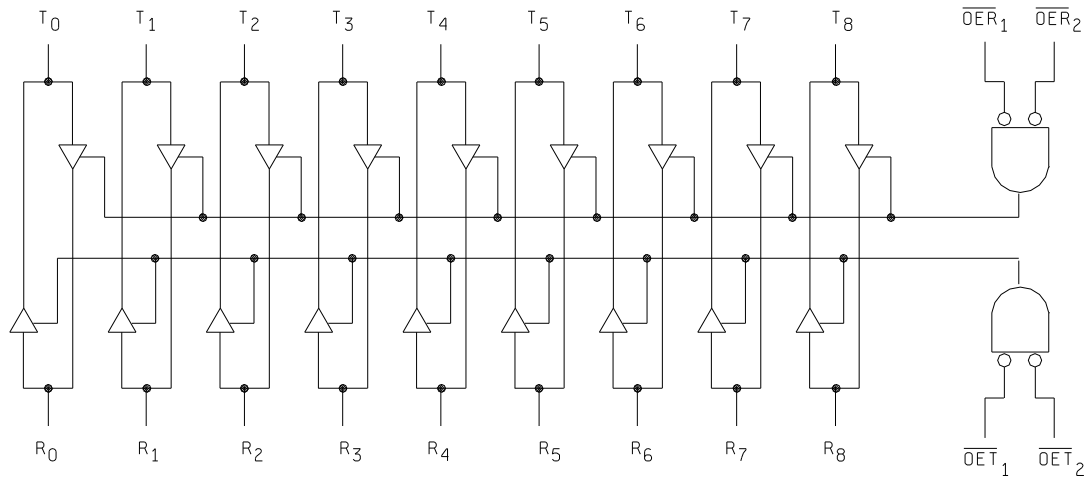


FIGURE 3. Logic diagrams.

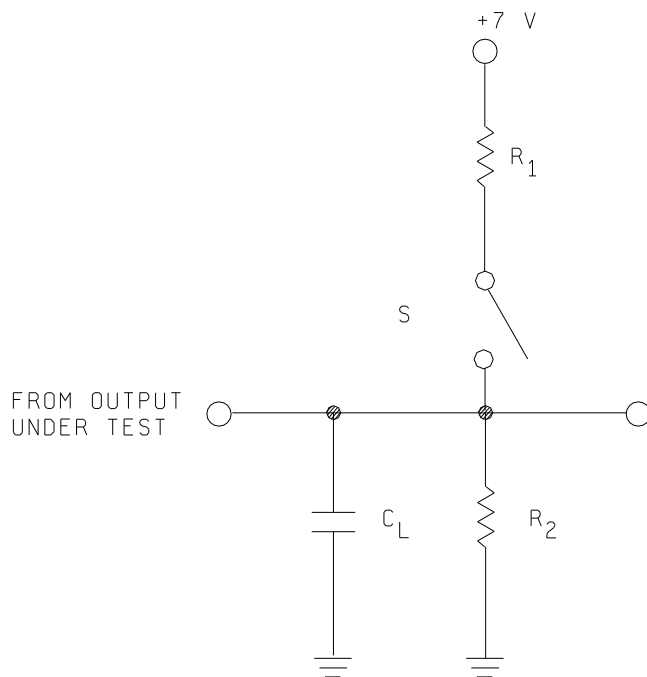
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Parameter	S position
t_{PLH}	Open
t_{PHL}	Open
t_{PHZ}	Open
t_{PZH}	Open
t_{PLZ}	Closed
t_{PZL}	Closed

Switch positions for
parameter testing

Load circuit for
three-state outputs

FIGURE 4. Switching circuits and waveforms.

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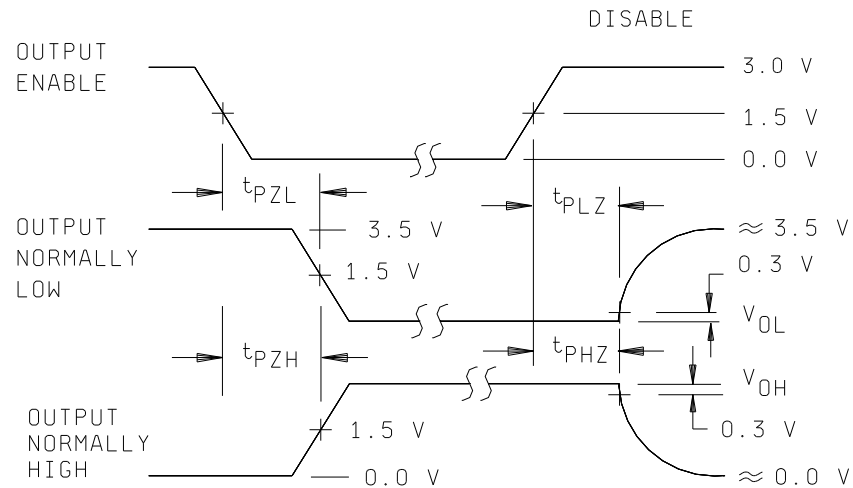
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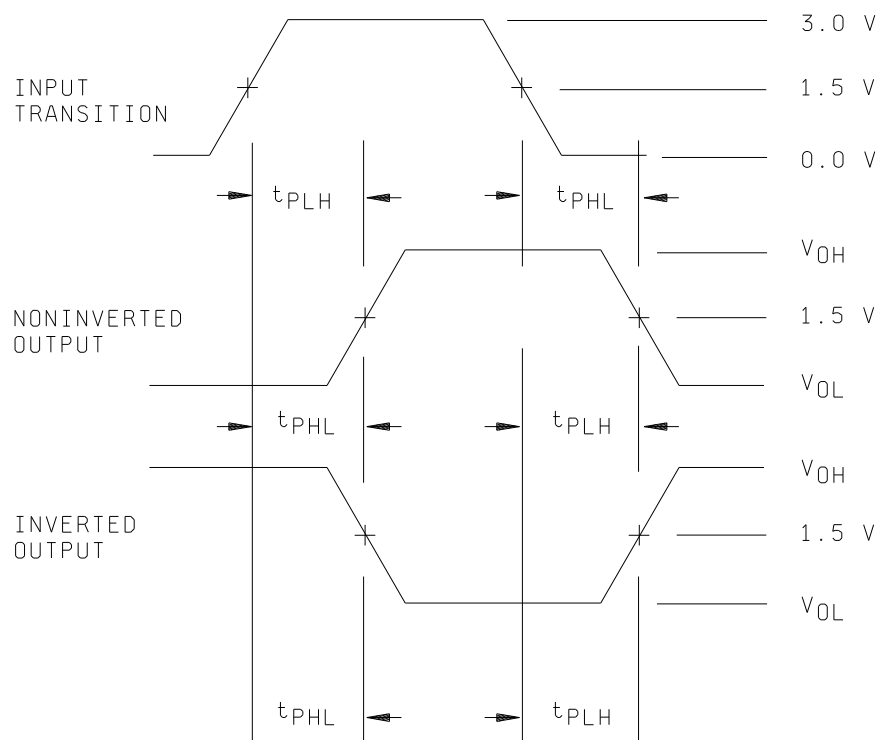
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Enable and disable times



Propagation delay



FIGURE

4.

Switching circuits and waveforms - Continued.

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3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall include the requirements for inputs, outputs, biases, and power dissipation, as applicable, in accordance with the specified purpose of method 1015.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9,10,11
Group A test requirements (method 5005)	1,2,3,4,7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1 and 7.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} , C_{OUT} , and $C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.
- d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE:

Approved sources of supply for SMD 5962-87704 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-8770401LX	34335	AM29C861/BLA
5962-8770401KX	34335	AM29C861/BKA
5962-87704013X	34335	AM29C861/B3A
5962-8770402LX	34335	AM29C863/BLA
5962-8770402KX	34335	AM29C863/BKA
5962-87704023X	34335	AM29C863/B3A
5962-8770403LX	<u>2/</u>	AM29C961/BLA
5962-8770404LX	<u>2/</u>	AM29C963/BLA
5962-8770405LX	34335	AM29C861A/BLA
5962-8770405KX	34335	AM29C861A/BKA
5962-87704053X	34335	AM29C861A/B3A
5962-8770406LX	34335	AM29C863A/BLA
5962-8770406KX	34335	AM29C863A/BKA
5962-87704063X	34335	AM29C863A/B3A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Not available from an approved source of supply.

Vendor CAGE
number

Vendor name
and address

34335

Advanced Micro Devices, Incorporated
901 Thompson Place
P.O. Box 3453
Sunnyvale, CA 94088

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